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ROBERT BLAU

Productive Knowledgeable Innovative

CAREER SUMMARY

Expert in design, development, and delivery of high performance, cost-effective computation and communication solutions. Experienced in all facets of project development: innovation, technical analysis, planning, design, implementation, delivery, and support. Excellent organizational, budget management, leadership, team building, and project management qualifications.

A career spent innovating, championing, and implementing new technologies to improve the capabilities, performance, and differentiation of products. Examples of innovations include: applying converged Ethernet to real-time applications, design and development of the first switched-PCI ASIC, applying switched-PCI to blade servers, and using Reed-Solomon encoding to provide error correction for an entire 16 bit wide DRAM component failure.

SKILLS

High performance system design

- Network convergence over 10/40Gb Data Center Ethernet
  - Ethernet protocols and standards
  - FCoE and IBoE technologies
  - Switch and NIC roadmaps
- Cluster and I/O interfaces
  - PCIe - Gen 2 and Gen 3
  - MPI, RDMA, Open Fabrics, I/OAT
- Accelerator architectures and limitations
  - FPGA's and GPGPU's
  - OpenCL programming
- SMP interconnects
  - QPI and HyperTransport
  - Multicore programming
- Intel and AMD Processor roadmaps

H/W development

- System Verilog, VHDL, Modelsim/Questasim
- Design tools: Xilinx, Altera, ASIC's, Boards

Software development

- C, Python, C++, Ruby
- Perl, Javascript, Bash
- LAMP development
- Linux, SVN, Bugzilla

Algorithm development

- Matlab
- Simulink, Sysgen

PROFESSIONAL EXPERIENCE

Mercury Computer Systems, Inc., 2004-2009 — Chelmsford, MA
Consulting Engineer

- Network/Storage/IPC/IO convergence over Layer 2 Ethernet
  Innovated the use of Data Center Ethernet as a transport layer for reliable, low latency, high bandwidth, inter-processor communication and streaming I/O. Modeled and optimized the latency, bandwidth, and reliability characteristics. Lead development of an FPGA design to implement the protocol.

- Future technology analysis
  Worked closely with CTO researching the use of 40Gbit Ethernet, Intel QPI, and PCI Express Gen 3 in future products.

- Software Defined Radio algorithm design and FPGA implementation
  Developed a Software Defined Radio application in an FPGA in only two months. Used Matlab, Simulink, and Sysgen to implement and deliver a working bitstream. Modeled the proprietary transmitter and receiver algorithms in Matlab, simulated the generated FPGA code in Simulink to validate correct frequency response, and successfully co-implemented the design in hardware.

- Serial RapidIO and DDR2 IP ASIC development
  Successfully designed and implemented IP to provide Serial RapidIO and SDRAM memory interfaces for a many-core ASIC, developed as part of DARPA's Polymorphous Computer Architecture Program. Innovated the application of Reed-Solomon encoding to provide complete error correction and recovery in the event of an entire 16 bit wide DDR2 SDRAM component failure.

- TI DSP board debug and support
  Successfully designed and implemented Serial RapidIO, SRAM, and 1 Gigabit Ethernet interfaces in an FPGA on a TI DSP board. Implemented a quick and simple Ethernet switch for the three DSP's to share one Ethernet port.

Mindstream Computing, Inc. 1998-2004 — Nashua, NH
Co-founder, CTO

- RapidIO to AMBA Bridge ASIC development
  Designed and co-implemented IP to bridge between the ARM AMBA bus and RapidIO.

- Radar emulator FPGA and board development
  Designed and delivered a programmable PCI board capable of emulating dozens of different types of radar data streams. No respin needed.

- RapidIO to PCI-X Bridge ASIC development
  Architected and co-implemented an ASIC to bridge between PXI-X and RapidIO.

- PCI-based blade server study for HP Labs
  Prepared a detailed study of the issues involved in the design of blade servers. Identified and provided analysis of configuration, addressing, interrupt, and hot swap issues.

Mercury Computer Systems, Inc. — Chelmsford, MA
Senior Systems Architect

- Blade server architecture and development
  Architected and directed the implementation of one of the first blade server systems to use a PCI switched fabric on the backplane.

- PCI switch architecture and development
  Innovated and developed my idea to connect PCI buses transparently through a switched fabric. Architected and co-implemented an ASIC to solve PCI connectivity limitations by emulating a hierarchy of transparent PCI to PCI bridges (with an option to do non-transparent bridging) through crossbar switches.

- Raceway Spec author and Chair for ANSI standardization

  Wrote the ANSI/VITA 5 Raceway Interlink switched fabric specification. Chaired the ANSI/VITA 5 standard committee and marshaled the specification through the ANSI standardization process at the VME Trade Association (VITA.)

- FPDP FPGA and board development

  Designed and delivered one of the first Front Panel Data Port boards for real-time streaming IO. Provided input for the standardization of the ANSI/VITA 17 FPDP specification.

Amdahl Corp. — Rexburg, ID
Systems Architect — Sunnyvale, CA

- Processor and System architecture, reporting to CTO

  Worked closely with the CTO and Chief Scientist as an advocate for change in both processes and products. Lead project studying trade-offs between pipeline levels, cycles per instruction, clock skew, and process variation to minimize cycle times. Researched ultra-high speed serial data links and ring structures for system connectivity. Developed a graphical performance modeling workbench in Smalltalk. Took a Vitesse GaAs ASIC design course.

- HW Design Manager

  Managed the development of a service processor (SVP) for IBM compatible mainframes. The SVP was a complex system consisting of an ECL barrel processor, memory and IO subsystem, running a modified UNIX kernel. Directed over 10 engineers in the development of ASIC's, board and backplane layout, software tools, microcode, simulation, and bring-up. Project was brought in on schedule with excellent morale and no turnover despite serious schedule and morale problems before I came on board.

- RTOS design

  Programmed major parts of the real-time operating system for a microprocessor-based diagnostic processor for IBM compatible mainframes. Also developed the communication hardware and software for this subsystem.

EDUCATION

University of California — Berkeley, CA
Graduate study, EE and CS

Massachusetts Institute of Technology — Cambridge, MA
BS, EECS

PUBLICATIONS

Converged Real-time Ethernet

Bob Blau, Ian Dunn, "*Using Layer 2 Ethernet For High-Throughput, Real-Time Applications*", High-Performance Embedded Computing (HPEC) Conference – Lincoln Labs, September 24, 2008
http://www.ll.mit.edu/HPEC/agendas/proc08/Day2/36-Day2-Session4-Blau-abstract.pdf
http://www.ll.mit.edu/HPEC/agendas/proc08/Day2/21-Blau-Presentation.pdf

PCI Switching

Bob Blau, Barry Isenstein, "*Improving PCI Connectivity*", Design SuperCon: High Performance System Design Conference, 1995

Bob Blau, Barry Isenstein, "*A Transparent Switching Fabric For PCI*", Real-Time Magazine, 96/4 - P.57

Bob Blau, Mike Maas, "*Improving PCI Scalability*", PCI-SIG Developers Conference, 1996

Bob Blau, Barry Isenstein, "*A Transparent Switching Fabric for PCI*", Hot Interconnects IV, Aug. 15-17, 1996, pages 215-219.

http://www.mc.com/uploadedFiles/pci-swtchng-fab-tb.pdf

Raceway Interlink ANSI Standard
http://ph-dep-ese.web.cern.ch/ph-dep-ese/crates/standards/Av5dot1.pdf